Journal of Power Sources 195 (2010) 1149–1155

Contents lists available at ScienceDirect

Journal of Power Sources

journal homepage: www.elsevier.com/locate/jpowsour

Fabrication and electrochemical performance of thin-film solid oxide fuel cells with large area nanostructured membranes

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ARTICLE INFO

Article history:
Received 7 July 2009
Received in revised form 24 August 2009
Accepted 25 August 2009
Available online 1 September 2009

Keywords:
Solid oxide fuel cell (SOFC)
Lanthanum strontium cobalt iron oxide (LSCF)
Yttria-stabilized Zirconia (YSZ)
Thin film
Micro-fabrication
Microstructure

ABSTRACT

Thin-film solid oxide fuel cells (SOFCs) with large (5-mm square) membranes and ultra-thin $La_{0.6}Sr_{0.4}Co_{0.8}Fe_{0.2}O_{3-\delta}$ (LSCF) cathodes have been fabricated and their electrochemical performance was measured up to 500 °C. A grid of plated nickel on the cathode with 5–10 μm linewidth and 25–50 μm pitch successfully supported a roughly 200-nm-thick LSCF/yttria-stabilized zirconia/platinum membrane while covering less than 20% of the membrane area. This geometry yielded a maximum performance of 1 mW cm^{-2} and 200 mV open-circuit voltage at 500 °C. Another approach toward realizing large area fuel cell junctions consists of depositing the membrane on a smooth substrate, covering it with a high-porosity material formed *in situ*, then removing the substrate. We have used a composite of silica aerogel and carbon fiber as the support, and show that this material can be created in flow channels etched into the underside of a silicon chip bonded to the top of the SOFC membrane. We anticipate these integrated fuel cell devices and structures to be of relevance to advancing low-temperature SOFCs for portable applications.

1. Introduction

Much research on solid oxide fuel cells (SOFCs) is currently focused on reducing the operating temperature below approximately 600 °C, to enable easier operation and compatibility with a wider range of materials [1,2]. Some efforts focus on exotic materials for the electrolyte and electrodes; others use thin-film deposition techniques to dramatically reduce the thickness of the membrane electrode assembly. Submicron-thickness membranes have been shown to enable reasonable power densities at lower temperatures [3–6], but it remains challenging to produce these membranes with areas large enough to be technologically relevant. In this paper we discuss two approaches for achieving large active areas, and the structural and electrochemical properties of cells made with each technique. We show that a roughly 200-nm-thick SOFC membrane can be stabilized over a 5-mm square area while covering less than 20% of the membrane area. Such an area is large enough to scale up by repetition, covering over 60% of the area of a large substrate with active SOFC membranes.

Thin-film solid oxide fuel cell electrolytes have been made by sputtering [3,6,7], electron beam evaporation [7], pulsed laser deposition [4], spray pyrolysis [4], and atomic layer deposition [5]. In most cases yttria-stabilized zirconia (YSZ) is used, although in some instances a layer of gadolinia-doped ceria (GDC) is used either alone [8] or added to YSZ on the cathode side to improve oxygen reduction kinetics [3]. Attempts have been made to deposit these electrolytes, as well as thin-film electrodes, on thick but porous substrates [9], an extension of the conventional electrode-supported SOFCs. However, this approach has difficulty simultaneously achieving both a dense electrolyte and a high concentration of electrochemically active sites. An alternative is to deposit the membrane on a thick substrate with a smooth surface, then selectively remove much of the substrate to expose the membrane [3,5–7]. The challenge in this case is that a large area of submicron-thick membrane is fragile, and must be supported at frequent intervals by a structural material with thickness intermediate between the membrane and the substrate. In addition, thin-film electrodes may have insufficient electronic conductivity to conduct current over macroscopic distances, in which case the support material must function as a current collector as well. One previous report exists of a grid of nickel metal used for this purpose, and describes structural and electrical properties of the device, with brief mention of electrochemical properties [10]. In that case, the substrate (silicon wafer) was several hundred microns thick, the membrane 700–900 nm thick, and the support grid, consisting of 10-μm-wide lines spaced by up to 80 μm, was 4–6 μm thick.

A number of reports indicate that the maximum freestanding width of a submicron SOFC membrane tends to be in the range of tens to a few hundred microns [3–5,7,11], less than the thick-

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doi:10.1016/j.jpowsour.2009.08.066

ness of most practical substrates. In some versions of fuel cells deposited on a flat substrate which is later removed, the support structure is useful to aid fabrication, because it can be difficult or expensive to etch high-aspect-ratio structures through the substrate, hence it is preferable if this etch step involves only coarse patterning. High-aspect-ratio structuring may also impede reactant and product diffusion, leading to degraded cell performance. In other versions, the support structure is not only useful but essential to convert a large fraction of the substrate area into active membrane. If an electrode material is to be deposited on the back side of the membrane after etching, then an etch technique with sloped sidewalls should be used in order to allow sufficient electrode material to reach the membrane surface. Given such sloped sidewalls, the area occupied by an each etch hole at the bottom of the wafer will be substantially larger than the active area exposed at the top, thus the total percentage of wafer area which can be made into active membrane, without supporting material, will be quite small.

For KOH etching through ⟨1 0 0⟩ silicon, a square active area with side w requires a square etch hole with side $w + t\sqrt{2}$ for a wafer thickness t, so the total active area can be no larger than $A_{active} = A_{wafer}(1 + t\sqrt{2}/w)^{-2}$. For a 500-μm-thick wafer with an active area width of 100 μm, for example, this gives $A_{active} = 1.5\%\ A_{wafer}$. Using a support grid, the active area covered by the grid must be considered as well, leading to $A_{active} = A_{wafer}(1 - l/p)^2(1 + t\sqrt{2}/w)^{-2}$ where l is the linewidth of the grid material and p is the pitch of the grid, but now w can be substantially larger. For example, increasing w to 5 mm but adding a grid with 5 μm linewidth and 50 μm pitch gives $A_{active} = 62\%\ A_{wafer}$, a 40-fold improvement despite cutting the size of freestanding regions in half. Additional improvements, such as thinner wafers and a technique we describe below for increasing grid thickness while consuming less active area, can increase the utilization further. The key is that in most cases, the lateral extent of the support material is comparable to its thickness, and a plated grid can be far thinner than the substrate. In both cases, real cell geometries will lose more active area than this, from edge exclusions, bonding regions, and areas dedicated to gas flow, for example. However, it is clear that a grid support yields tremendous advantages relative to support by the substrate alone. The first design we study in this paper contains a nickel grid deposited on the cathode side of the membrane. We show that this grid successfully stabilizes a 180-nm-thick $La_{0.6}Sr_{0.4}Co_{0.8}Fe_{0.2}O_{3-\delta}$ (LSCF)/YSZ/porous Pt membrane over a 5-mm square area and gives an open-circuit voltage (OCV) and maximum power density up to 202 mV and 1 mW cm^{-2} at 500 °C.

A second option to support a submicron membrane is to essentially reverse the conventional electrode-supported geometry: deposit the membrane on a smooth substrate, cover it with a porous material, and then remove the substrate. The ideal porous support would have high diffusivity and a pore size substantially smaller than the maximum allowable freestanding membrane width. It should adhere to the membrane surface without wetting and blocking too many active sites, possess sufficient mechanical strength to counteract film stresses generated during either deposition or heating to the operating temperature, and be stable itself at high temperatures under possibly changing oxidative environments. Further desirable properties of this material include electrical conductivity (so that it can function as a current collector) and catalytic activity—the large surface area of such a porous material may serve as a scaffold for catalyst particles, for example for internal reforming reactions to occur directly in the anode chamber. Here we focus on the mechanical properties and demonstrate the concept using a silica aerogel reinforced with carbon fibers, formed *in situ* between the membrane surface and a silicon cover piece.

2. Experimental procedures

2.1. Grid-supported membranes

Fig. 1 shows the lithographic processes used to form grid-supported membranes. We have reported on the structure and electrochemical performance of cells with identical membrane materials, thicknesses, and deposition parameters in detail elsewhere [6,11,12] but without the support materials necessary to form large area membranes. We begin with a silicon wafer coated on both sides with 200 nm of low pressure chemical vapor deposition (LPCVD) silicon nitride. 80 nm of 8 mol% YSZ and 20 nm of LSCF are sputtered onto the top surface. Both films are deposited at 1 nm min^{-1} from oxide targets, in 5 mT of argon with the substrate held at 500 °C. A bilayer of resist is then spun onto the sample, LOR-3A lift-off resist (Microchem Corp.) first, followed by S1813 photoresist (Rohm and Haas Co.), baking the layers at 170 °C and 115 °C, respectively. The resist is exposed with the grid pattern, and the S1813 is developed in CD-30 (Rohm and Haas Co.) and baked at 140 °C. The LOR is then etched in CD-26 (Rohm and Haas Co.) just long enough to reach the LSCF surface but no longer, to avoid significant undercutting. A physical mask is then placed over the chip, covering the edges, while a thin (∼100 nm) nickel seed layer is sputtered onto the surface, as shown in Fig. 1(a). Now the photoresist is dissolved in acetone, lifting off the unwanted nickel seed material but leaving the LOR layer intact. The chip is then immersed in electroless nickel plating solution (Nickelex, Transene Corp.) at 88 °C to plate 5–10 μm of nickel, as shown in Fig. 1(b). The LOR layer is dissolved in Remover PG (Microchem Corp.), then the back side nitride is patterned via reactive ion etch (RIE) using a mixture of CF_4 and O_2 through a physical mask, followed by etching through the wafer in 30 wt% KOH at 96 °C (Fig. 1(c)). During this etch the chip is sealed into a stainless steel housing with o-rings to ensure that KOH only touches the bottom of the chip. Finally, the silicon nitride on the back side and underneath the membrane is removed with another RIE step, and a 0–60 nm blanket coat of YSZ is sputtered onto the back side (as previously but at room temperature) followed by a porous Pt anode (sputtered at room temperature in 75 mT of argon). The completed device is shown schematically in Fig. 1(d).

This patterning procedure for the nickel grid accomplishes several goals. First the nickel plating solution can slowly etch LSCF. Thus, the LOR protects the LSCF over what will become active mem-

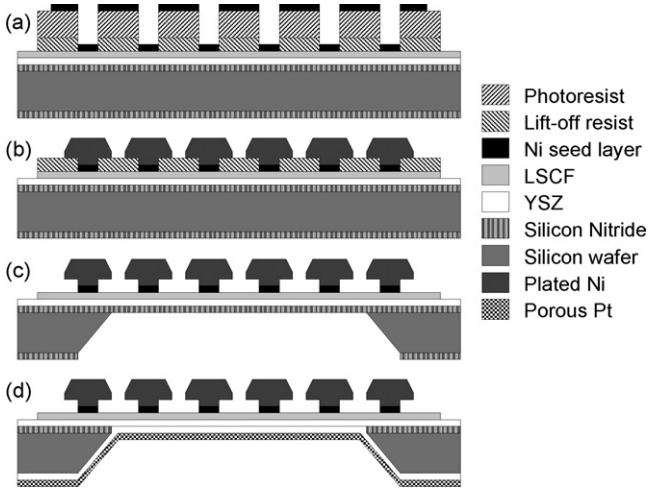

Fig. 1. Top side grid process: (a) after deposition of YSZ, LSCF, and patterned nickel seed layer; (b) photoresist is lifted off and nickel is plated; (c) LOR is removed and the wafer is etched through; (d) additional YSZ may be coated on the back side, followed by the porous Pt anode.

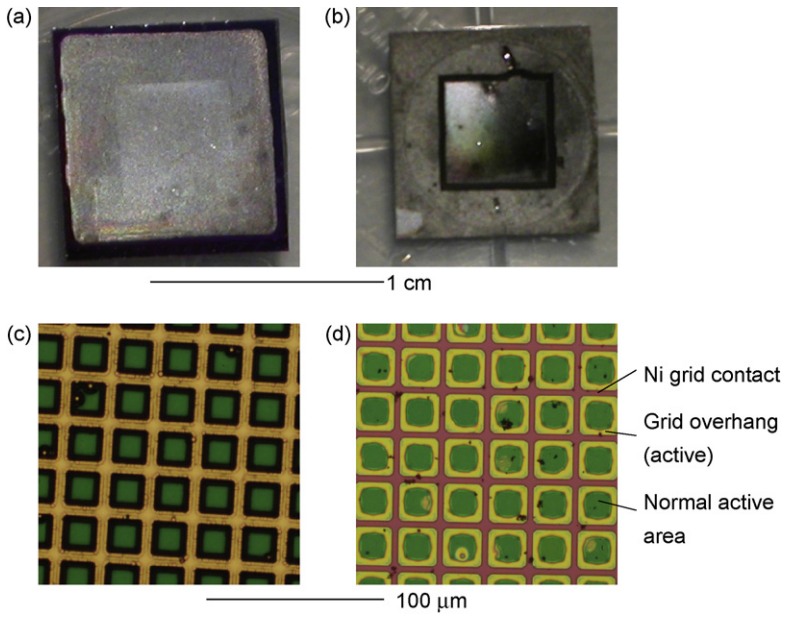

Fig. 2. Top side grid devices: (a) top view and (b) bottom view of an entire completed chip; (c) top view and (d) bottom view of the grid just before Pt deposition.

brane areas, and undercutting of this layer (which would lead to a gap between LOR and nickel seed coverage) should be minimized. Second, with no nickel seed near the edge of the chip, LSCF is removed there, minimizing the possibility of electrical shorts from Pt that may deposit up the side of the chip. Third, the thickness and therefore strength of the nickel grid may be increased without usurping additional active membrane area. Because plating is roughly isotropic, the grid lines grow outward as well as upward during plating, but due to the LOR layer, the LSCF is still exposed to gas underneath this overhang. In the present devices a relatively thin (~300 nm) LOR layer was used, which may inhibit diffusion as the overhang may be as much as 10 μm wide, but a thicker LOR layer could be used as well.

Fig. 2 shows several optical images of a grid-supported membrane device, either completed (Fig. 2(a) and (b)) or after KOH etching but prior to the final RIE step (Fig. 2(c) and (d)). In Fig. 2(a) the entire chip is shown from above, with the active area visible as the lighter square in the center. The edge exclusion, where no nickel seed layer was deposited thus the LSCF was partially etched, is the dark border. In Fig. 2(b) we see the same chip from below, coated with porous Pt on the unpolished, unetched bottom edge of the wafer, down the sloped sidewalls of the KOH etch (dark), and on the active area in the center. Zooming in, Fig. 2(c) shows the result of plating roughly 5 μm of nickel onto a 25-μm-pitch, nominal 5-μm-linewidth grid pattern. The nickel is relatively flat (bright area) over approximately 5 μm but then slopes down (dark area) for a total width of 13 μm. In addition, occasional spontaneous plating nucleation sites can be seen, covering part of the active area with unwanted nickel. From this image alone it would appear that this grid has covered over 75% of the membrane area. However, the bottom view, Fig. 2(d), shows another advantage of the LOR layer: the actual nickel grid lines in contact with LSCF are only about 3 μm wide and cover only 22% of the active area. The rest of the nickel is lifted off the LSCF surface, which alters the color of reflected light due to interference effects. The spontaneous nucleation sites can also be seen, generally lifted slightly higher off the surface, but close to flat on the bottom, as evidenced by the interference patterns.

The amount of active area covered by the grid lines could be further decreased by increasing the grid pitch at constant linewidth, however with the currently used process parameters a 25-μm grid is more reliable than a 50-μm grid, although no chips have emerged from processing completely defect-free. Out of eight chips each with 25-μm and 50-μm grids with nominal 5-μm linewidths, aside from two in which the grid peeled off, the number of visible cracks in the membranes ranged from two to about a dozen on the 25-μm chips, and about a dozen to a few hundred on the 50-μm chips (out of 40,000 grid cells on each 25-μm chip and 10,000 on each 50-μm chip).

Most of the cracks occur either during the RIE nitride removal or during porous Pt deposition, both of which increase compressive stress on the membrane [12], however nearly all membrane failures we have observed coincide with visible grid defects, either cracks or errors in lithography. Fig. 3(a) shows two cracks in a 25-μm grid (horizontal, bottom center, and vertical, just left of center). Zooming further in, it is clear from the continuity of globular plating structures across the cracks that these occurred after plating was finished. Fig. 3(b) shows the same region, but focused on the membrane rather than the top of the grid, showing that from each grid crack there are membrane cracks extending to the next unbroken gridline, where they stop. Presumably the vertical membrane crack extends below the horizontal gridline, but is shadowed by the overhang of the vertical gridline. Fig. 3(c) shows a region of 50-μm grid with a single crack in the center. The buckling of unbroken membranes, extending 3 or 4 cells to either side of the crack, shows that the diagonal pointing toward the crack is shortened, indicating that the crack in the gridline was created to relieve tensile stress in the nickel, while the membranes, with their compressive stress, adapt to the shapes taken on by the grid.

2.2. Gel-supported membranes

Fig. 4 shows the process used to form aerogel-supported membranes. The assemblies are formed from two chips, a top and a bottom piece, both starting as 10-mm square silicon chips coated on both sides with 200 nm of low pressure chemical vapor deposited (LPCVD) silicon nitride. The top chip, when bonded to the bottom, will serve as a flow channel for air and a container for the aerogel. A large square of nitride is removed from one side of the top chip and two long slits from the other, followed by etching in KOH from both sides until the etch holes meet mid-wafer, as shown in Fig. 4(a).

The bottom chip is coated with YSZ and LSCF and a hole opened in the back side nitride as described above. An adhesion layer of Cr

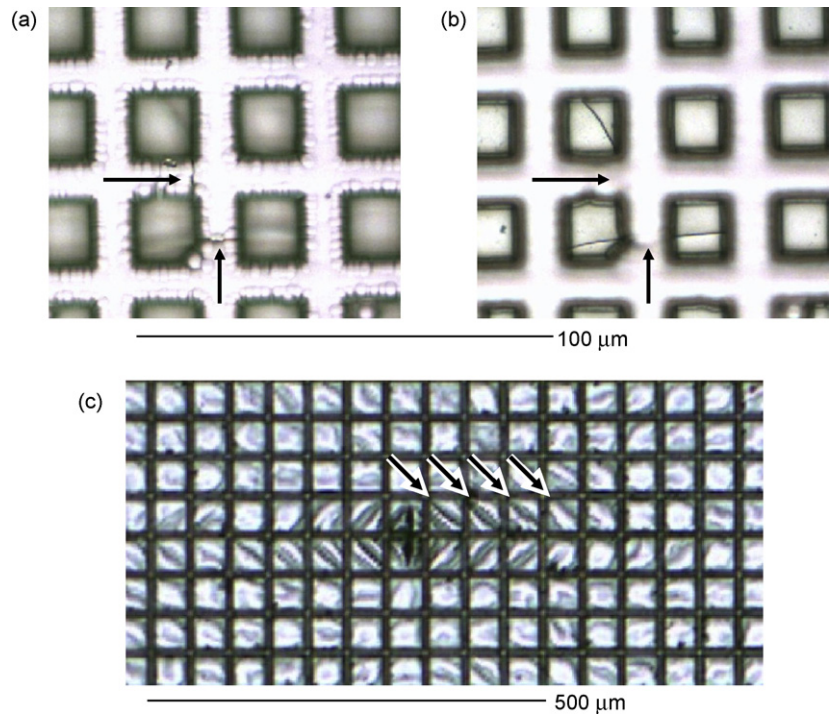

Fig. 3. Defects in the top side grid. Focusing on the (a) top of the grid and (b) top of the membrane around a set of grid defects. Arrows at the same positions in both images indicate the grid defects. (c) Deformation of the grid around a defect evidenced by buckling patterns of the membranes. Arrows indicate one of the four series of diagonally buckled grid cells, above right of the defect.

and a bonding layer of Au is electron-beam evaporated onto the top of the bottom chip, masked to deposit only around the edge where the two chips will be bonded, as shown in Fig. 4(b). The remaining silicon nitride is removed from the top chip with phosphoric acid (85% in water, heated to 180 °C) and the same Cr/Au bonding layer is evaporated to its bottom surface, after which the chips are bonded together in an EV Group Inc. EV501 wafer bonder, at 350 °C and 1000 N for 30 min at 10^{-5} torr. The resulting structure is shown in Fig. 4(c). The top chip serves as a container for the aerogel. This leaves an open space inset into one side of the top chip in which the aerogel is located, accessible by two slits on the other side for gas inlet and outlet.

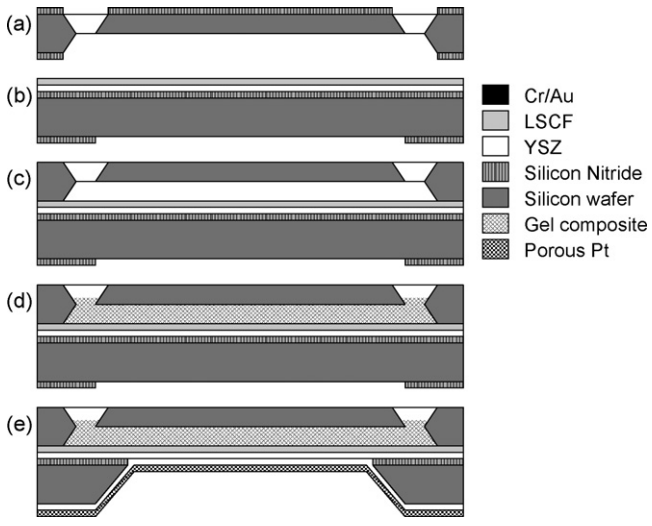

Fig. 4. Gel support process: (a) YSZ, LSCF, and patterned gold bonding layer are deposited, and the etch mask is patterned into the back side; (b) a second chip, etched to form a gas flow channel, is bonded on top; (c) carbon fiber aerogel composite is formed in the flow channel; (d) the device is completed similarly to the grid process.

The next step is to fill the space between the top and bottom chips with a porous medium, as shown in Fig. 4(d). Silica aerogels were synthesized in a two-step acid–base catalyzed process following Ref. [13] and described below. We point out that other types of aerogels such as carbon aerogels synthesized with resorcinol and formaldehyde and used with fiber support as electrodes in supercapacitors could be suitable as well due to their electronic conductivity [14]. Also, the recently demonstrated carbon nanotube aerogels [15] may be ideal for this purpose. In these gels, polyvinyl acetate (PVA) is used to strengthen the gels, with the disadvantage that it decreases electrical conductivity, however at SOFC operating conditions the PVA may pyrolyze and enhance its conductivity. The gels are formed as a composite with carbon fiber, as a key criterion of this process is low shrinkage of the gel after gelation, and several authors have found that forming the gel as a composite with larger fibers accomplishes this [16,17].

To form the gel/fiber composite, milled carbon fiber (Toho Tenax Co.) is manually packed into the two-chip fuel cell assembly with a thin rectangular foil until the space is filled. Commercially available prepolymerized tetraethyl orthosilicate (Silbond Corp., H5), ethanol, water, and NH_4OH (30% in H_2O) were mixed in a 1:1.7:1.5:0.007 volume ratio then directly pipetted into the fuel cell assembly containing carbon fiber. The mixture is left in ethanol-saturated air to gel for 1 h, and then submerged in a bath of water, ethanol, and 30% NH_3/H_2O in a 1:1:0.003 ratio for 18–24 h to age the gel. Ethanol replacement, then CO_2 replacement follows to prepare the gel for supercritical drying with CO_2, which minimizes capillary forces during drying. Supercritical drying is performed in a custom-built autoclave, constructed from a 2″ ID steel elbow as a pressure chamber, fed by a siphon-type carbon dioxide cylinder, submersed in a water bath connected to a recirculating thermoelectric temperature controller.

After the gel is dried, the structure is completed using the same processing steps as in the grid devices: KOH etching, nitride removal, optional YSZ deposition, and porous Pt anode deposition. The only difference is that RIE, despite coming from the opposite

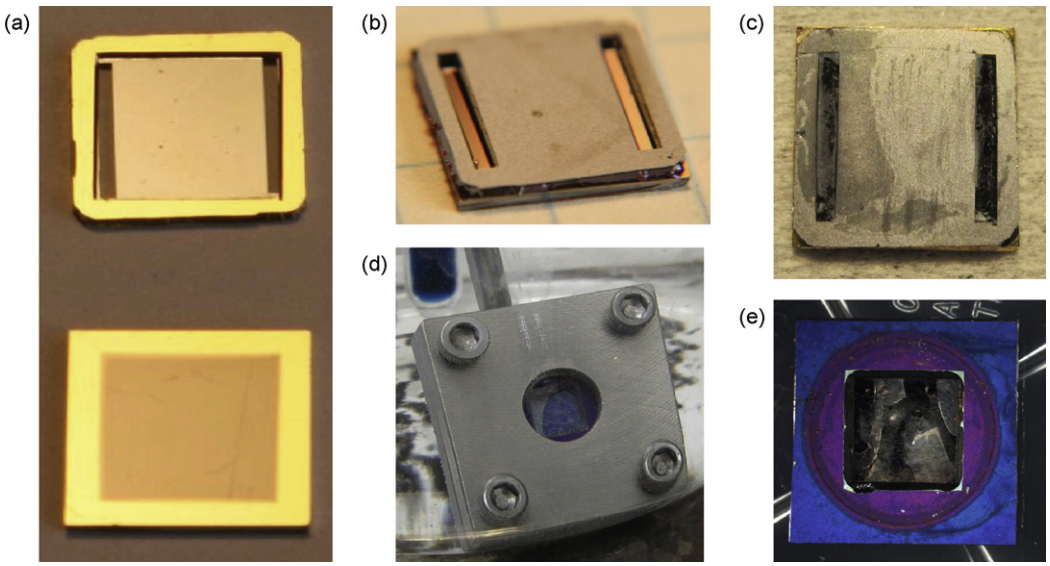

Fig. 5. Gel device images—top and bottom chips: (a) ready for bonding and (b) after bonding; (c) after injection and drying of the fiber/gel composite; (d) near the end of KOH etching; (e) after etching a device with only silica aerogel, no carbon fibers, the debonded, broken, and shrunken gel can be seen through the membrane.

side of the chip, could cause significant damage to the nanofibers of the aerogel, so the back side nitride is instead removed by wet etching in phosphoric acid, while the top and sides of the device are still protected inside the stainless steel housing.

Fig. 5 shows the gel-supported devices at various processing steps. Fig. 5(a) shows the two chips ready to be bonded, with the cathode side flow channel and inlet and outlet slits etched into the top chip and the YSZ and LSCF layers on the bottom, along with Cr/Au bonding layers on each chip. The chips are then bonded (Fig. 5(b)), and filled with fiber/gel composite (Fig. 5(c)). The darker regions in the slit are fiber/gel composite, while the lighter are pure silica gel on top of the fibers. Non-reinforced silica aerogels we make with the same precursor concentrations have a density of around 0.1 g cm^{-3}. In these devices we measure approximately 0.05(±50%) g cm^{-3} of silica gel (approximately 3% filling) and 0.4 g cm^{-3} of carbon fiber (approximately 20% filling), giving a total porosity of around 75–80% for the composite.

Fig. 5(d) shows a chip pair in KOH, protected by the stainless steel housing. At the top one can see a stainless steel tube which is welded into the back of the protective housing and extends upward out of the KOH, venting the protected side to prevent pressure changes across the membrane due to the temperature of the bath. In this image, the etch is nearly complete, with a little silicon remaining on upper left of the membrane, and the fiber/gel composite can be seen in the remainder. Finally, Fig. 5(e) shows a device after etching through the silicon wafer but before removing the silicon nitride layer. This device was made with only silica aerogel, no carbon fiber, and it is clear that the gel has shrunk tens of percent in linear dimension and is not bonded to the membrane. The nitride is strong enough, however, that while it is present even as a large membrane does not necessarily break. From Fig. 5(c) and (d) it is clear that the fiber/gel composite exhibits little or none of the shrinkage that hampered the gel-only device in Fig. 5(e). Another gel composite fabrication route, mixing the carbon fiber and aerogel precursors prior to injection between the bonded chips, was found to yield too low a density of fibers to provide this mechanical stability.

3. Electrochemical performance

Fig. 6 shows the electrical performance of a representative grid-supported device, with a 5-mm square active area and a 50-μm nickel grid. The observed open-circuit voltages (V_{OC}) were low enough (maximum 202 mV at 500 °C) that the *I–V* curve at any given time was essentially a straight line connecting the open-circuit and short-circuit conditions. This reflects the fact that with a low V_{OC}, the current produced by the cell is substantially less than the internal leakage current, thus the activation overpotential is essentially constant due to its logarithmic dependence on current. Also, in a situation like this we significantly oversupply reactants to the cell, such that concentration losses do not arise, and only linear contributions remain in the current–voltage relationship. Each *I–V* curve can then be described by two parameters; namely V_{OC} and area-specific resistance (ASR), but others can be calculated: short-circuit current $I_{SC} = V_{OC}/R_M$ peaks at 19 mA cm^{-2} at 500 °C, and maximum power $P_{max} = I_{SC}V_{OC}/4$ reaches 1.0 mW cm^{-2}.

To interpret these data, we can model the device with the circuit equivalent shown in Fig. 7, including an electrochemical voltage

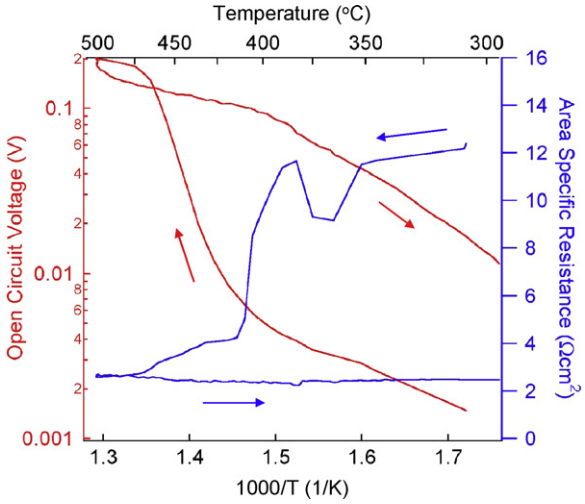

Fig. 6. Electrical performance of a grid-supported device. Open-circuit voltage (red curve, left axis) and area-specific resistance (blue curve, right axis) vs inverse temperature. The Celsius equivalent is shown on the top axis. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

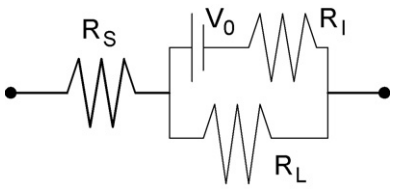

Fig. 7. Linearized equivalent circuit model used to analyze grid-supported device performance.

source V_0 in series with an ionic resistance R_I, a leakage resistance R_L due to electronic connection (short circuit) between the electrodes, and a series resistance R_S due to contacts and current collection. In this linearized, low-V_{OC} model, V_0 would not be the theoretical cell potential but due to the non-linearity of activation potentials should be around 0.5–0.7 V for this structure, based on extrapolations of our previous measurements [6]. R_L accounts for defects in the membrane that allow the Pt anode to contact either the Ni grid or the LSCF cathode, either at a visible crack or at a microscopic defect such as a pinhole. Such contact could occur during deposition, if for example the Pt deposits conformally through a crack; after deposition, if displacement due to a crack causes the cathode to contact an adjacent region of anode; or by diffusion, if during heating Pt atoms migrate through a pinhole or crack to form a bridge between the electrodes. This model leaves out gaseous leaks and the distributed nature of the series resistance, but it is useful for qualitative interpretation. Gas leaks are less likely to contribute significantly to the low-V_{OC} we observe, as they would lead to a concentration profile, and consequently V_{OC}, relatively independent of temperature. Within this model the measured open-circuit voltage would be $V_{OC} = V_0/(1 + R_I/R_L)$, and the area-specific resistance, $ASR = R_S + R_I R_L/(R_I + R_L)$.

In a well-functioning fuel cell, the ASR would be dominated by R_I (activation overpotential is primarily combined into V_0) with a much larger R_L and a much smaller R_S. However, the small V_{OC} indicates that $R_I > R_L$. From our previous work with these identical membrane materials [6] we expect a maximum power in the order of 60 mW cm^{-2} at 500 °C at around 0.3 V, implying an R_I around 1.5 Ω cm^2. In order to create the observed V_{OC} then, R_L should be around 0.75 Ω cm^2.

This leaves the majority of ASR (approximately 2 Ω cm^2 after heating) to be taken up by R_S. Possible sources of series resistance include current collection effects, such as partial etching of LSCF around the edges of the nickel grid or interface oxidation between the LSCF and nickel, as well as contact and lead resistance. We could also account for this ASR via higher device and leakage resistance if the intrinsic membrane performance (without leakage) were on the order of 3 mW cm^{-2}, substantially lower than our previous devices but possible if, for example, the edges of the LSCF etched sufficiently to disconnect a substantial fraction of the membranes from the current collector grid.

Various features seen in Fig. 6 support a number of conclusions about device characteristics. First, V_{OC} shows an overall trend toward higher values at higher temperatures, which is to be expected since V_{OC} is determined, as described above, by the ratio of ionic to leakage resistance, and the ionic conduction is thermally activated. However, no single activation energy may be extracted. Various slopes are seen, corresponding to activation energies around 0.43 eV in heating up to 400 °C, 0.22 eV cooling from 500 °C to 400 °C, and 0.8 eV cooling below 400 °C. An apparent activation energy of 3 eV is seen during the rapid performance improvement around 450 °C in heating, however this is likely related to a change in morphology of one or more layers of the membrane. Although the LSCF and YSZ were deposited at 500 °C and thus are expected to already be crystalline, the improvement at 450 °C suggests that one or both of these layers required further structural transformation to achieve better electrochemical performance. One likely explanation is that oxygen deficiency during deposition led to incomplete crystallization of the LSCF. A final salient feature of the V_{OC} data is the slowing and ultimate reversal of its rise as we approach 500 °C. We have observed such degradation in previous work [6] although generally at somewhat higher temperature and manifest in maximum power rather than V_{OC}. We attribute this effect most likely to agglomeration of the Pt anode. For this reason, no data were taken above 500 °C as this would have led to further degradation.

The ASR data in Fig. 6 exhibit two distinct drops. Aside from some noise between 350 °C and 400 °C, there is a rapid drop just above 400 °C, and another smoother decline around 450 °C coinciding with the steep rise in V_{OC}. As ASR is a function of R_S (in addition to R_I and R_L which appear in V_{OC}) and the first drop does not correspond to any clear feature in V_{OC}, we attribute this drop to a decrease in R_S, likely an improvement in contact resistance to the measurement circuit. The second drop corresponds to a decrease in R_I upon crystallization. The near constancy of ASR after these two events over a wide temperature range provides further evidence that it is dominated by R_S, with R_I and R_L substantially smaller thereafter. Taken together, these data show that the key element to focus on in improving the performance of these devices is the leakage resistance R_L, without which V_{OC} and power production would improve dramatically.

4. Conclusion

In this paper, we have examined two approaches for strengthening a large area of thin-film solid oxide fuel cell membrane, such that it could be scaled up. The first technique, using a plated grid, has been demonstrated to preserve the integrity of the vast majority of sub-membranes and produce power. The second technique involves strengthening with a porous layer of aerogel/carbon fiber composite fabricated *in situ*, also compatible with microfabrication. We anticipate these approaches to be of potential relevance in scaling up low-temperature SOFCs for portable or intermittent power applications.

Acknowledgments

We thank the staff at the Rowland Institute at Harvard for technical support. The authors acknowledge financial support from SiEnergy Systems, the Harvard University Center for the Environment, and the Eppley Foundation for Research.

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